

30.6 A 10dB 44GHz Loss-Compensated CMOS Distributed Amplifier

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Growing demand for high-speed communication channels, capable of transferring high volume of data in real time, is the driving force for the telecommunication industry to expand the optical networks closer to customers' home and businesses. Developing low-cost optical transceivers accelerates the deployment of all-optical networks by reducing the overall cost of the optical networks. Deep submicron CMOS technology has a lower fabrication cost and a higher level of integration compared with conventional high-speed semiconductor technologies (GaAs, SiGe, InP, and GaN). Although lagging behind compound semiconductor technologies, the intrinsic speed of Si MOSFETs has significantly improved, owing to aggressive scaling of the technology that makes it a viable choice for the implementation of high-speed broadband communication circuits. This paper focuses on the implementation of broadband amplifiers; the fundamental building blocks of high data-rate optical telecommunication systems in CMOS technology.

Distributed amplification is widely used as a circuit topology for achieving a flat gain and good input and output matching over a very large bandwidth. As shown in Fig. 30.6.1, distributed amplifiers (DAs) are constructed of 2 transmission lines (TLs) that connect the gate and drain terminals of the transistors. These TLs are realized in CMOS using the top-most and thickest metal layer either in the form of spiral inductors, microstrip TLs, or coplanar waveguides. In any case, because of semiconductive nature of the silicon substrate and limited resistivity of the metal layers, they dissipate power in the substrate and metal layers. The substrate loss increases with frequency as the substrate coupling increases and substrate resistance decreases. The metal loss also rises with frequency as more current flows through the outer layers of the metal interconnects (skin and proximity effect). Lossy TLs dissipate some of the incident power as signal travels from the input to the load. If the TL losses are increasing with frequency, the power gain of the TL is decreasing accordingly. This is the reason that a sloping gain versus frequency is reported in many recent works on CMOS DA [1-3]. Shigematsu et. al. [4] presented an RC degenerated common-source gain cell to provide a flat gain within the amplifier's bandwidth. Although this method proves successful in flattening the gain, the proposed source-degenerated transistor reduces the gain by a factor of $1+g_m Z_{\text{Source}}$ resulting in a small gain of 4dB for the DA.

To compensate for the loss of the TLs, an alternative approach that is not in direct trade-off with the gain of the amplifier is proposed. Compensating the loss of each TL individually by using shunt negative resistors is presented. Figure 30.6.2 shows single-stage circuit diagrams of four lossless, lossy, loss-compensated, and high-frequency loss-compensated TLs and their corresponding power gains as functions of frequency. As shown by square-marked line, an ideal TL provides a flat gain over its entire bandwidth. As ideal inductors are replaced by the on-chip spiral inductors, as expected the gain of the TL is significantly reduced as frequency increases (circle-marked line). Adding the frequency-independent shunt negative resistors will compensate the loss of the on-chip inductors, but changes the characteristic impedance of the TLs at lower frequencies, and therefore causes significant gain overshoot at low frequencies (up-triangle-marked line). To solve this issue, a capacitor is placed in series to the negative resistor to decouple the negative resistors from the TLs at low frequencies, achieving a flat gain over the entire DA Bandwidth (down-triangle-marked line).

Figure 30.6.3 illustrates several known circuit topologies that can produce a negative resistor: a common-gate transistor with an inductor connected to the gate, a cross-coupled differential pair, and a capacitively degenerated common-source configuration. Among these architectures, only the capacitively degenerated common-source configuration meets the constraint of isolation at low frequencies. The input impedance seen from the gate of the transistor is equivalent to a negative resistor with a value of $g_m/w^2 C_g C_s$ in series with 2 series capacitors, C_g and C_s . In addition, the frequency-increasing negative conductance is desirable because the losses of on-chip inductors can be compensated for a wide frequency band as their losses behave similarly with respect to the frequency. Since C_s blocks the DC current, a resistor is placed in parallel with this capacitor to provide the DC path required for biasing the common source transistor. The value of the biasing resistor must be several times larger than the impedance of C_s , and small enough to provide the DC current needed for producing the required g_m for compensating the loss of TLs.

On-chip octagonal inductors are used in this design. To achieve a 40GHz bandwidth and a 50Ω characteristic impedance simultaneously for the TLs, the value of inductors and capacitors of the gate and drain TLs are computed as 398pH and 159fF, respectively, according to the equations in Fig. 30.6.1. The sum of the parasitic capacitors of transistors and on-chip inductors at each node of the TL should not exceed the calculated value of 159fF. The gain fluctuation around the cutoff frequency is because of termination of the TL in a 50Ω load instead of its image impedance. Adding m-derived network at both ends of the TL can solve this problem. To reduce the capacitive coupling between the TLs and improve the reverse isolation of the amplifier, a cascode configuration is selected for the gain cells.

The 8-stage CMOS DA chip is laid out in an area of 0.6×2.5mm² as shown in Fig. 30.6.7. Because of unpredictable loss of the on-chip inductors when placed close to each other or to other metal interconnects, the DC biasing of the negative resistor circuit (V_{B2}) is separated from those of the TLs in order to provide the flexibility for alternating the power produced by the negative resistors for full loss compensation. Also, the gate DC bias for the cascode transistors is provided externally (V_{B1}). These 4 DC biases are provided through RF probes using T-bias connections (gate and drain TLs' DC biases) and using DC probes (V_{B1} and V_{B2}). At full compensation, the power consumption is measured 44mW and 59mW for the DA and loss compensation circuitry, respectively. Figure 30.6.4 shows S-parameters measured using on-wafer probing. The DA exhibits an average gain of 9.8dB with a gain variation from 8.6 to 10.6dB. The 3-dB and unity-gain bandwidths of the DA are 43.9 and 44.6GHz, respectively. The input and output return loss in better than -14dB and -8dB over the entire bandwidth, respectively. The reverse isolation is measured below -25dB. Figure 30.6.5 shows the measured noise figure of the DA which averages at 5dB ranging from 2 to 7dB. As summarized in Fig. 30.6.6, in addition to providing a large flat gain, the proposed amplifier exhibits a gain-bandwidth product comparable with those of the most recently published CMOS DAs.

References:

- [1] R.E. Amaya, N.G. Tarr, and C. Plett, "A 27 GHz Fully Integrated CMOS Distributed Amplifier Using Coplanar Waveguides," *RFIC Symp. Dig.*, pp. 193-196, Jun., 2004.
- [2] M. Tsai, H. Wang, J. Kuan, and C. Chang "A 70GHz Cascaded Multi-Stage Distributed Amplifier in 90nm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 402-403, Feb., 2005.
- [3] R. Liu, T. Wang, L. Lu, H. Wang, et al., "An 80GHz travelling-wave amplifier in a 90nm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 154-155, Feb., 2005.
- [4] H. Shigematsu, M. Sato, T. Hirose, et al., "40Gb/s CMOS Distributed Amplifier for Fiber-Optic Communication Systems" *ISSCC Dig. Tech. Papers*, pp. 476 - 540, Feb., 2004.

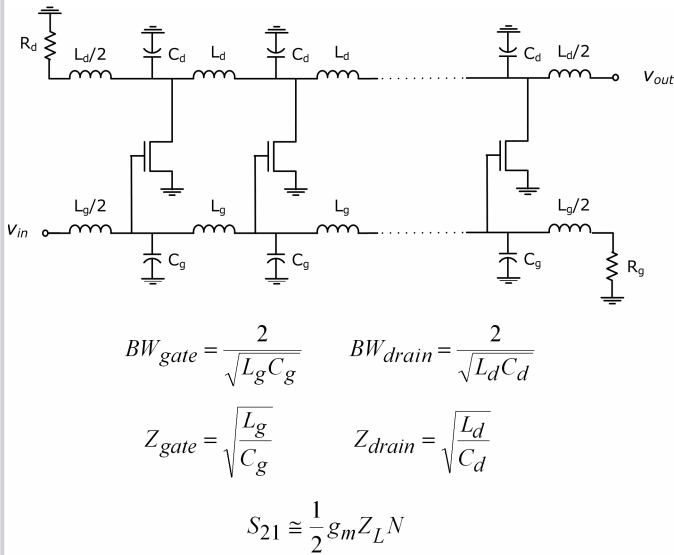


Figure 30.6.1: Schematic of the CMOS distributed amplifier.

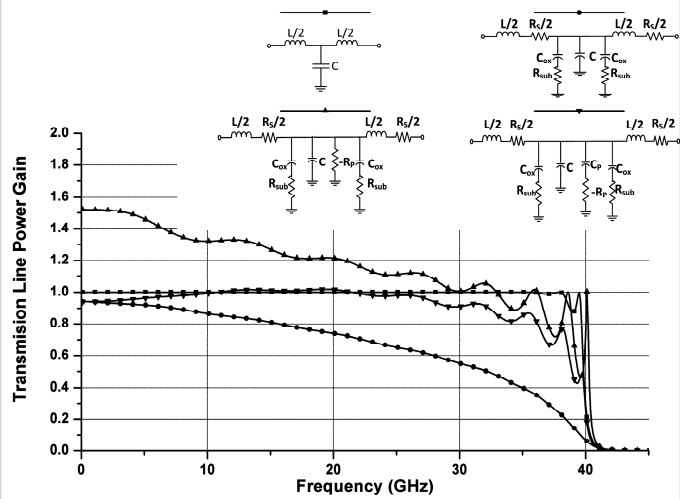


Figure 30.6.2: Schematic diagram and power gain of lossless, lossy, loss-compensated, and high-frequency loss-compensated TLs.

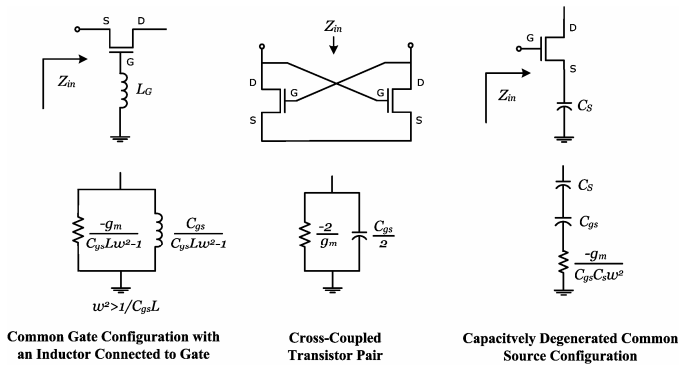


Figure 30.6.3: Known negative resistor implementations and their equivalent small-signal circuits.

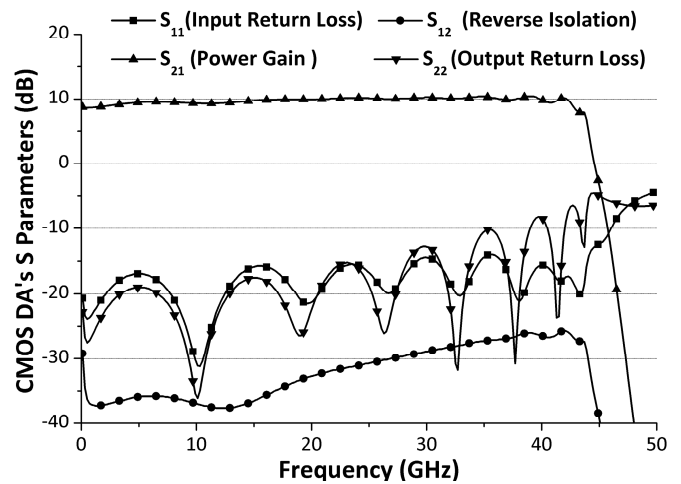


Figure 30.6.4: Measured S-parameters of CMOS DAs.

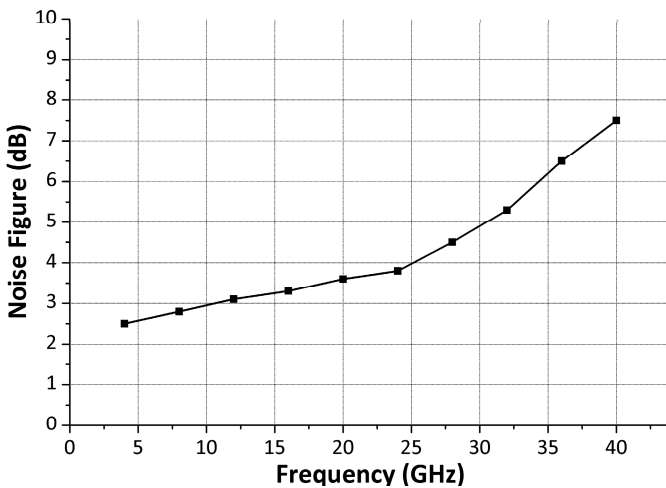


Figure 30.6.5: Measured noise figure.

Technology and [Ref]	Bandwidth (GHz)	Gain (dB)	Area (mm×mm)
0.18μm CMOS [1]	15	8	1.3×1.8
0.09μm CMOS [2]	70	7	0.9×0.8
0.09μm CMOS [3]	80	7.4	1.2×0.6
0.18μm CMOS [4]	39	4	1.1×3.0
0.13μm CMOS [This work]	44	10	0.6×2.5

Figure 30.6.6: Performance comparison of this work with recently published CMOS DAs.

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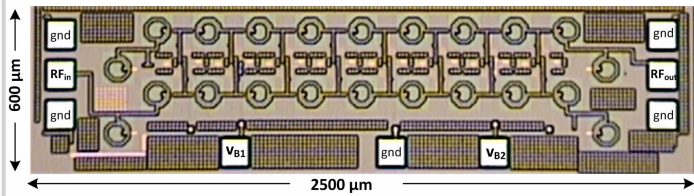


Figure 30.6.7: Die micrograph of proposed CMOS DA.